

WHAT IS CLAIMED IS:

1 1. A method of manufacturing a capacitor of a semiconductor
2 device, the method comprising the steps of:

3 i) sequentially depositing a first insulating layer, an etching stop layer,
4 and a second insulating layer on a semiconductor substrate;

5 ii) etching a predetermined portion of the second insulating layer to
6 form a preliminary hole for exposing the etching stop layer;

7 iii) forming a first hole by transversely expanding the preliminary hole
8 in the second insulating layer;

9 iv) forming a second hole by etching a predetermined portion of the
10 etching stop layer and the first insulating layer at a bottom surface of the first
11 hole, the second hole making contact with an electrode area of the
12 semiconductor substrate and having an area narrower than the first hole;

13 v) forming a first conductive layer pattern uniformly on sidewalls of the
14 first and second holes and on a bottom surface of the second hole; and

15 vi) sequentially depositing a dielectric layer and a second conductive
16 layer pattern on the first conductive layer pattern.

1 2. The method as claimed in claim 1, wherein the steps of forming
2 the first and the second holes comprise the substeps of:

3 a) providing a photoresist pattern for forming the preliminary hole
4 on the second insulating layer;

5 b) anisotropically etching the second insulating layer using the
6 photoresist pattern as an etching mask to form the preliminary hole and
7 exposing the etching stop layer;

1 c) isotropically etching a sidewall of the preliminary hole in the
2 second insulating layer to transversely expand the preliminary hold to form the
3 first hole; and

4 d) anisotropically etching a predetermined portion of the exposed
5 etching stop layer and the first insulating layer at the bottom surface of the first
6 hole using the photo-resist pattern as the mask to form the second hole and
7 expose the semiconductor substrate.

1 3. The method as claimed in claim 2, wherein a hole in the photo-
2 resist pattern is formed on a portion of the second insulating layer in an area
3 that corresponds to an upper center portion of the electrode area of the
4 semiconductor substrate.

1 4. The method as claimed in claim 2, wherein the first and second
2 insulating layers are etched at an etching selectivity ratio of 5-25 to 1 with
3 respect to the photoresist pattern.

1 5. The method as claimed in claim 2, wherein the anisotropic
2 etching with respect to the first and second insulating layers is carried out by a
3 dry etching process by supplying a mixed gas including C_5F_8 , O_2 , CH_2F_2 , Ar,
4 and CO at an appropriate combination of the gas components.

1 6. The method as claimed in claim 2, wherein the isotropic etching
2 with respect to the sidewall of the preliminary hole is carried out such that the
3 second insulating layer has an etching selectivity ratio of about 10-40 to 1 with
4 respect to the etching stop layer.

1 7. The method as claimed in claim 2, wherein the isotropic etching
2 with respect to the sidewall of the preliminary hole in the second insulating layer
3 is carried out by a wet etching process.

1 8. The method as claimed in claim 1, wherein the first and second
2 insulating layers are formed to a thickness in a range between about 100 and
3 about 1500 nm using materials having insulating and reflowing characteristics,.

1 9. The method as claimed in claim 1, wherein the etching stop
2 layer is formed by depositing a silicon nitride or a silicon oxy-nitride material.

1 10. The method as claimed in claim 1, wherein the etching stop
2 layer has a thickness in a range between about 5 and about 200 nm.

1 11. The method as claimed in claim 1, wherein the step of forming
2 the first conductive layer pattern comprises the substeps of:

3 a) depositing a first conductive layer on the sidewalls of the first and
4 second holes, on the bottom surface of the second hole, and on the second
5 insulating layer; and

1 b) etching back the first conductive layer until the second insulating
2 layer outside the first and second hole is exposed.

1 12. The method as claimed in claim 11, wherein the first conductive
2 layer has a thickness in a range between about 20 to about 200 nm.

1 13. The method as claimed in claim 11, wherein the etch-back step
2 is carried out by a dry etching process or a chemical mechanical polishing
3 process.

1 14. The method as claimed in claim 11, further comprising the step
2 of depositing a hemispherical silicon grain (HSG) layer on the first conductive
3 layer pattern which is deposited on the sidewalls of the first and second holes
4 and on the bottom surface of the second hole.

1 15. The method as claimed in claim 1, wherein after forming the first
2 conductive layer pattern, the second insulating layer is removed by a selective
3 etching process to expose both sides of the first conductive layer pattern above
4 the etching stop layer before depositing the dielectric layer and the second
5 conductive layer pattern.

1 16. The method as claimed in claim 15, further comprising the step
2 of forming a hemispherical silicon grain (HSG) layer on an entire surface of the
3 first conductive layer pattern.
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1 17. The method as claimed in claim 7, wherein the wet etchant is a
2 buffered oxide etchant (BOE).
3

4 18. The method as claimed in claim 8, wherein the materials used
5 for forming the first and second insulating layers are boro-phospho-silicate-
6 glass (BPSG) or undoped silicate-glass (USG).
7

8 19. The method as claimed in claim 11, wherein the first conductive
9 layer material is doped poly-silicon.
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11 20. The method as claimed in claim 15, wherein the selective
12 etching process is a wet etching process.
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14 21. The method as claimed in claim 11, wherein the etch-back
15 process is performed by a chemical mechanical polishing (CMP) process or a
16 dry etching process.

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